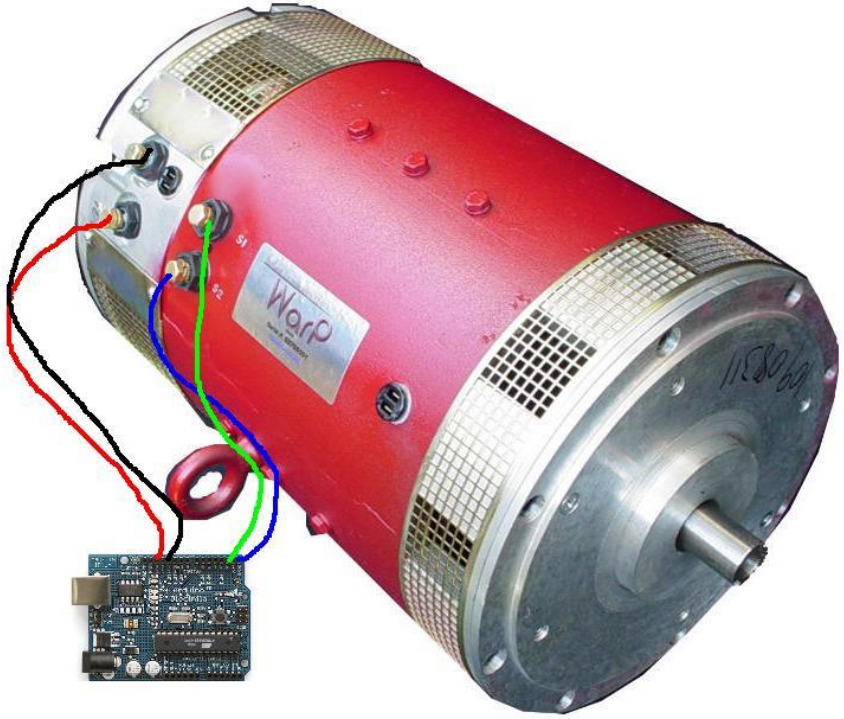
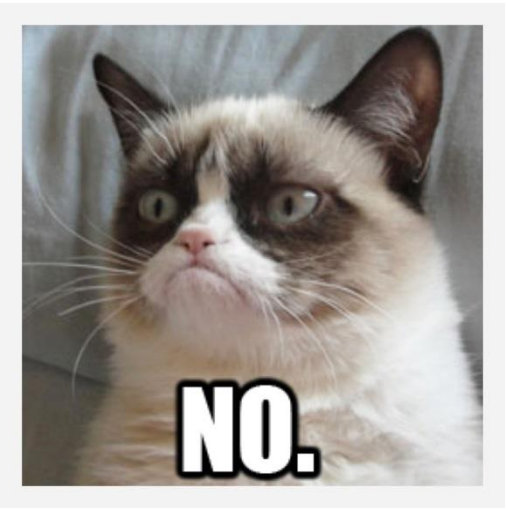
High-Powered Output Devices

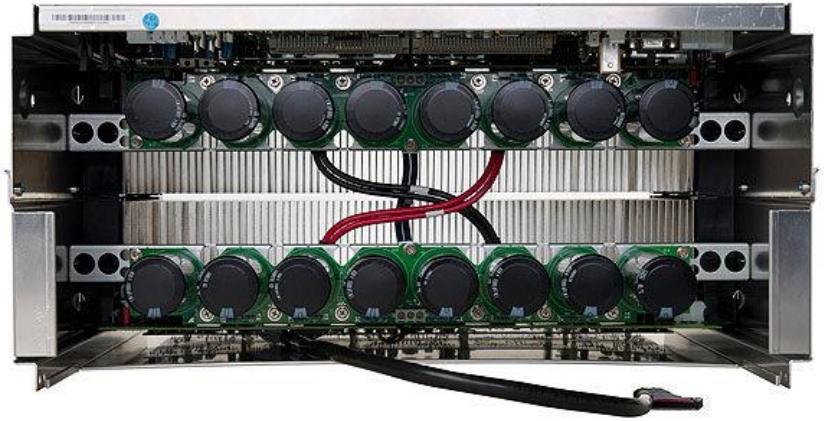


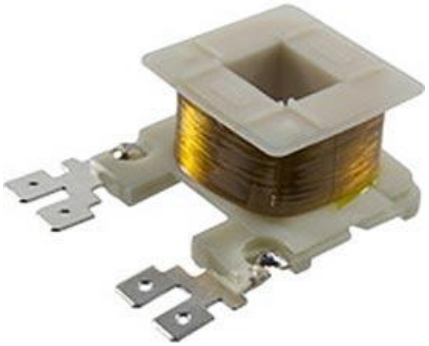


And How to Control Them

What is a High Powered Output Device?

- Typically an actuator or transducer
- Usually highly *inductive* in nature
- Usually powered by *switching* instead of *linear* (resistive) means
- Chief examples: Motors, speakers, relay coils; arrays of LEDs.
- Tens of Watts (to thousands of watts)
- General principles are good practice for all circuit powers.





Topics

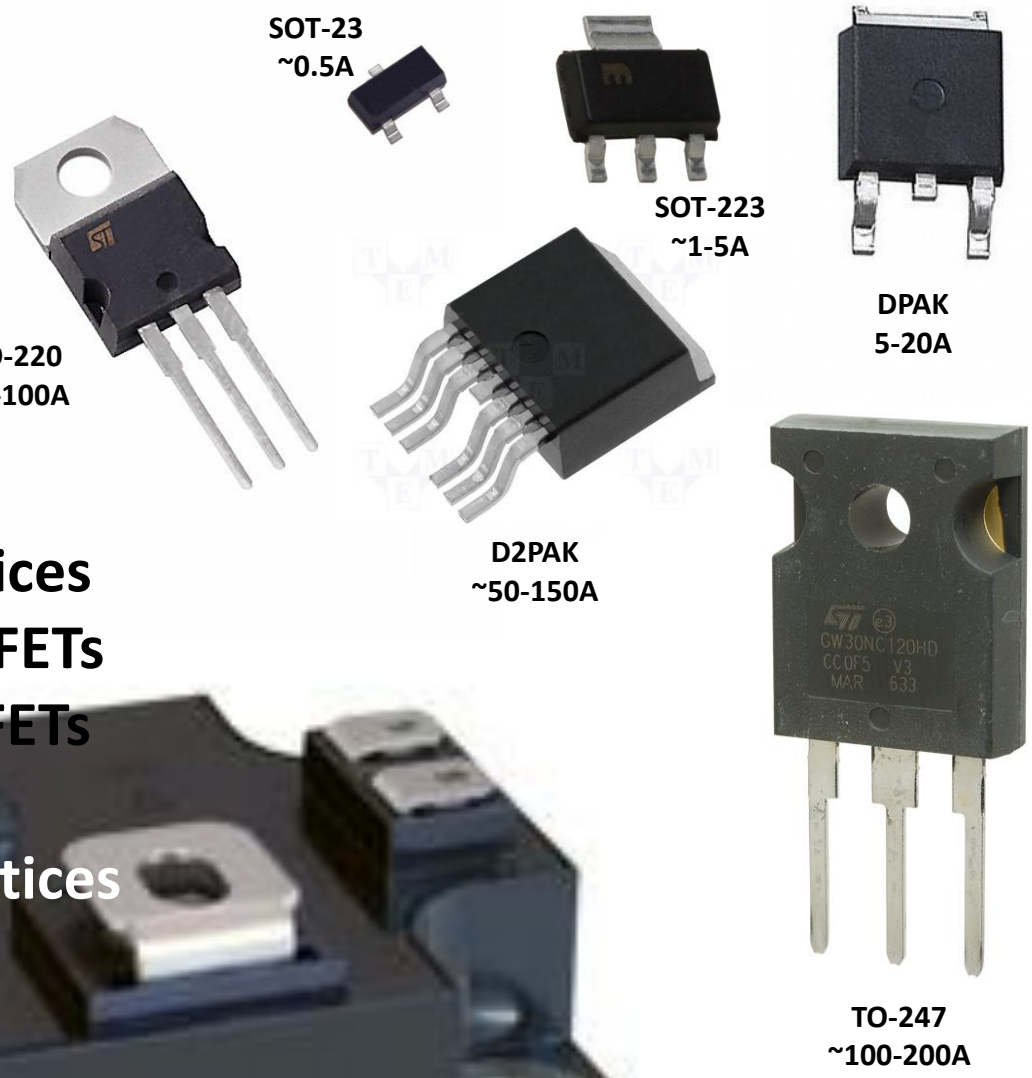
- About MOSFETs
- Output topologies
  - Low-side drive
  - High-side drive
  - Half-Bridge
- How to drive and use devices
  - Using N-channel MOSFETs
  - Using P channel MOSFETs

Gate Drivers

Circuit Board layout practices

- dI/dt and dV/dt
- Groundskeeping

Q&A, Discussion



Proprietary modules
100 – 1000+A

MOSFETs

- Why focus on them rather than BJTs ("transistors")? More modern, better suited for switching applications.
  - **BJTs are still common and useful in their own right**
- Things to know:
  - They drive like *capacitors* (**V_{gs}; C_{gs}**)
  - You must fill the capacitor > **$V_{th\ (reshold)}$**
  - They come in N and P types
  - **N: Vg > Vs** to turn on; **P: Vg < Vs**.
  - They can conduct in reverse (**Body Diode**)
  - They have a maximum voltage-across rating (**V_{ds}**) beyond which they will self-destruct (**Avalanche breakdown**)
  - They have a static on-resistance (**R_{ds}**)
  - For now, they can be simply modeled as a switch: you touching the two wires together.

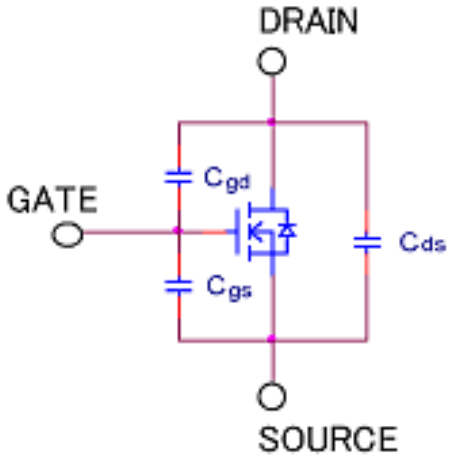
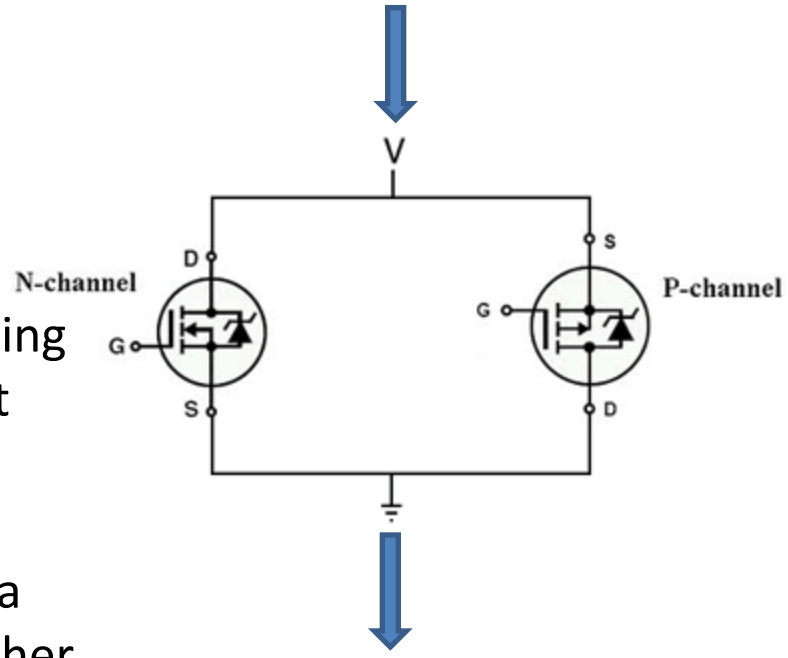


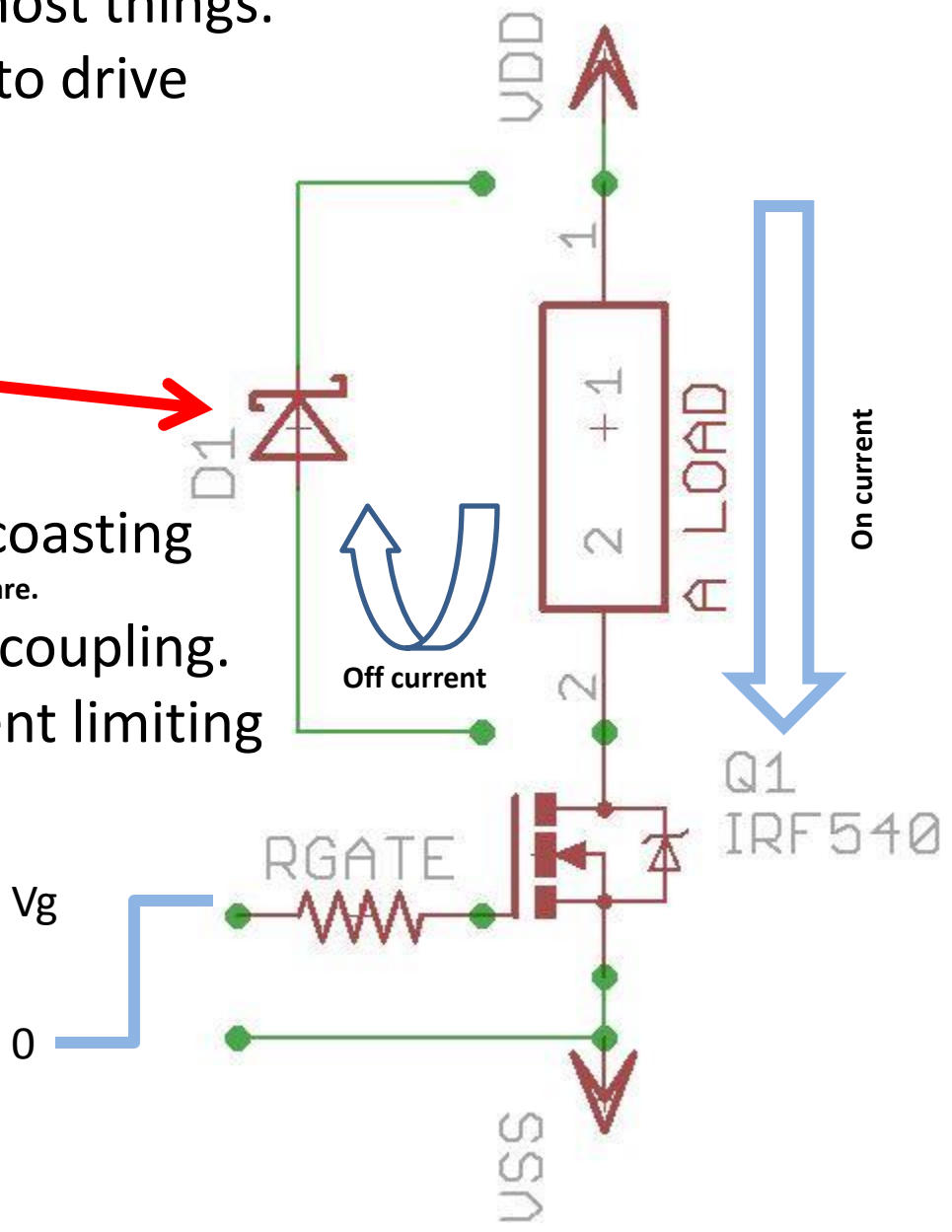
Figure 1:
MOSFET Capacitance Model



Output Topologies – Low-Side Drive

- Easiest to execute; works for most things.
- Ground-referenced, so “easy” to drive
  - $\mathbf{V_{gs}}$ where $\mathbf{V_s} = 0$
- Ideally, $\mathbf{V_g} >> \mathbf{V_{th}}$ for lowest $\mathbf{R_{ds}}$
- Inductive loads require a recirculating diode

- Motors: single direction only; coasting
  - This is all that very simple, cheap motor controllers are.
- Speakers: require capacitative coupling.
- LEDs: works great; needs current limiting e.g. using a resistor.



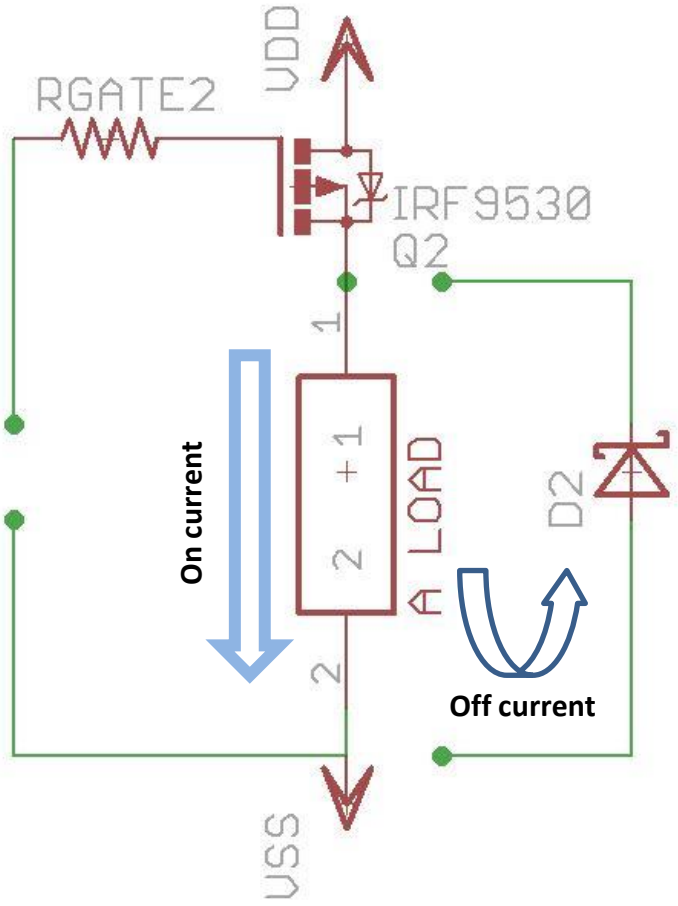
Output Topologies – High-Side Drive

- A P-channel device is used with Source at $\mathbf{V_{DD}}$ (most positive voltage)
- To turn on, pull Gate to $\mathbf{V_{SS}}$ (0v, ground)
  - This yields the $-\mathbf{V_{gs}}$ to turn it on.
- Pch devices have higher $\mathbf{R_{ds}}$ by nature
- $\mathbf{V_{DD}}$ must be less than $\mathbf{V_{gs,max}}$
- Often used to drive a bigger N-channel stage without a "gate driver" chip
- Conversely, is often driven **by** a tiny N-channel stage before this.

$\mathbf{V_{DD}}$

0

$\Delta\mathbf{V_g}$ MUST BE LESS THAN $\mathbf{V_{gs,max}}$
For most applications, this is < 20v
For logic level FETs, this could be < 10v
Your microcontroller pins are likely not happy with > 7v.



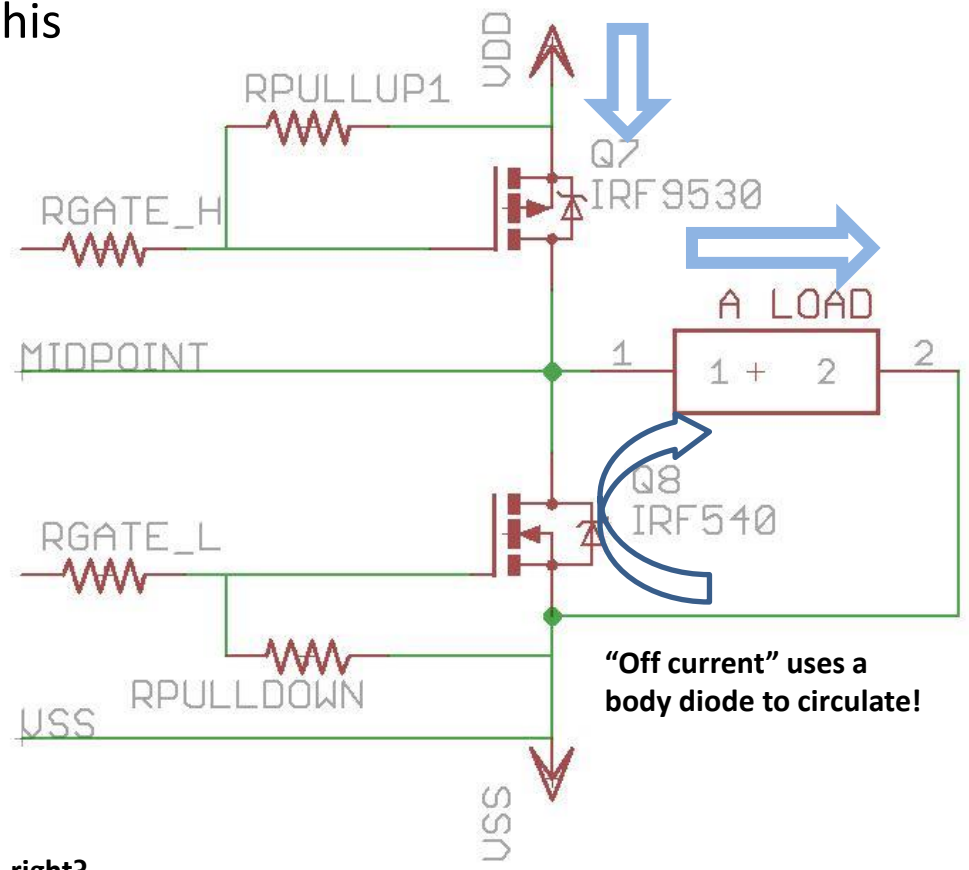
Output Topologies – Half-Bridge, P and N

- A *half bridge* topology is where a FET controls access to both $\mathbf{V_{DD}}$ and $\mathbf{V_{SS}}$
- Also called "Totem Pole" output
- P & N type combines relative ease of driving either side device with independent inputs.
- Usually limited to $\mathbf{V_{DD}} < 20v$
- Can be driven a few ways – more on this shortly.

Many low-cost motor controllers and amplifiers are made this way. It is common to find packaged P-and-N FETs together in one multi-pin device.

RGATE_H is usually pulled down directly to $\mathbf{V_{ss}}$ with a small N-channel FET driven by the microcontroller.

RGATE_L is usually driven directly by the microcontroller, or (conversely) driven using a small P-channel device for higher $\mathbf{V_{gs}}$.

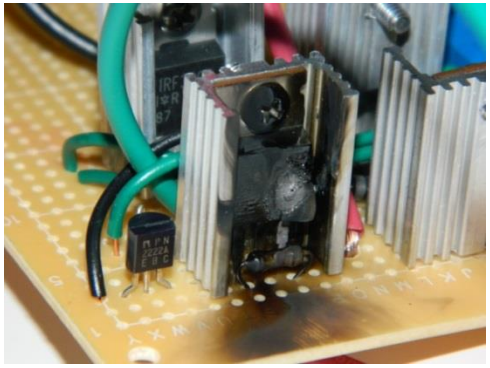


"Off current" uses a body diode to circulate!

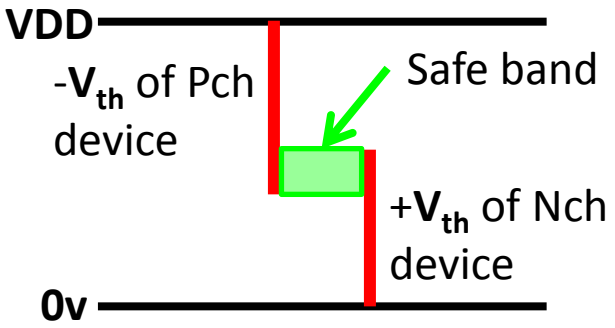
Funny how P and N channel devices seem to *complement* each other, right?

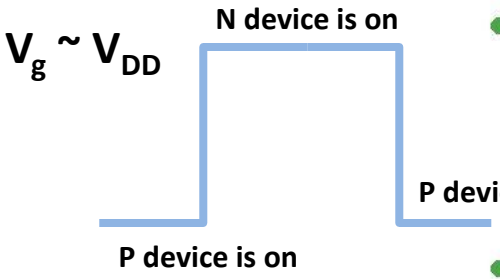
Output Topologies – Naïve Half-Bridge

- **This** is how everyone tries at first
- Not only are you limited to $\mathbf{V_{DD}} \sim \mathbf{V_{gs,max}}$
- But for anything but very low $\mathbf{V_{DD}}$s, you will get *shoot-through current*.
- "High = off" isn't failsafe.
  - Large $\mathbf{R_{pullup}}$ to keep Q3 off

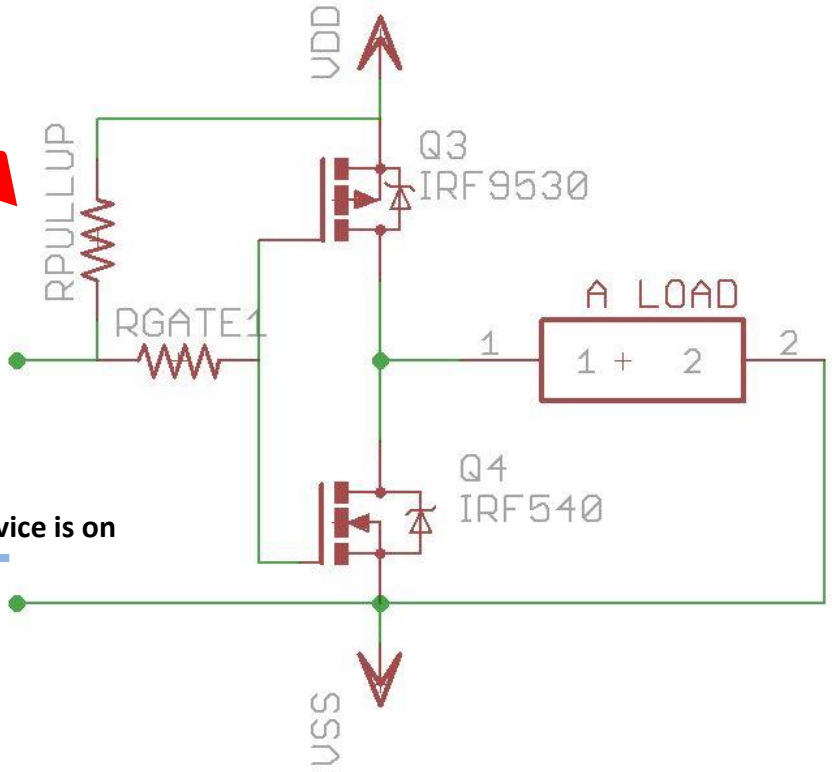


Shoot-Through will demolish your FETs faster than you can say "Neil Gershenfeld"





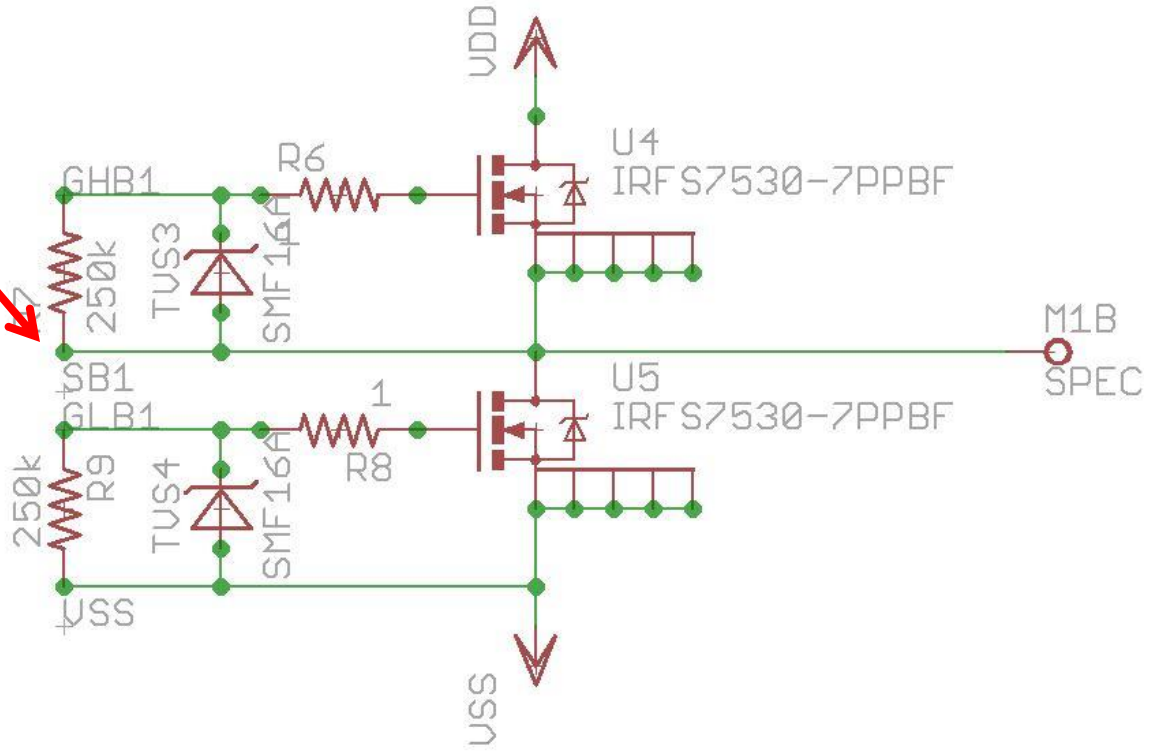
Shoot-through will occur if there is no **overlap** in the two $\mathbf{V_{th}}$ voltages when compared to VDD.



Output Topologies – All-N-Channel Half Bridge

- The preferred topology for modern switching power supplies, motor drivers, and Class-D amplifiers.
- N-channel means less losses
- But how to switch the high-side device? (since $V_s \approx V_{DD}$, hence $V_g > V_{DD} + V_{th}$)
- A "Greater than V_{DD}" supply has to exist.

$V_{sb1} \approx V_{DD}$ when "high side" is on…

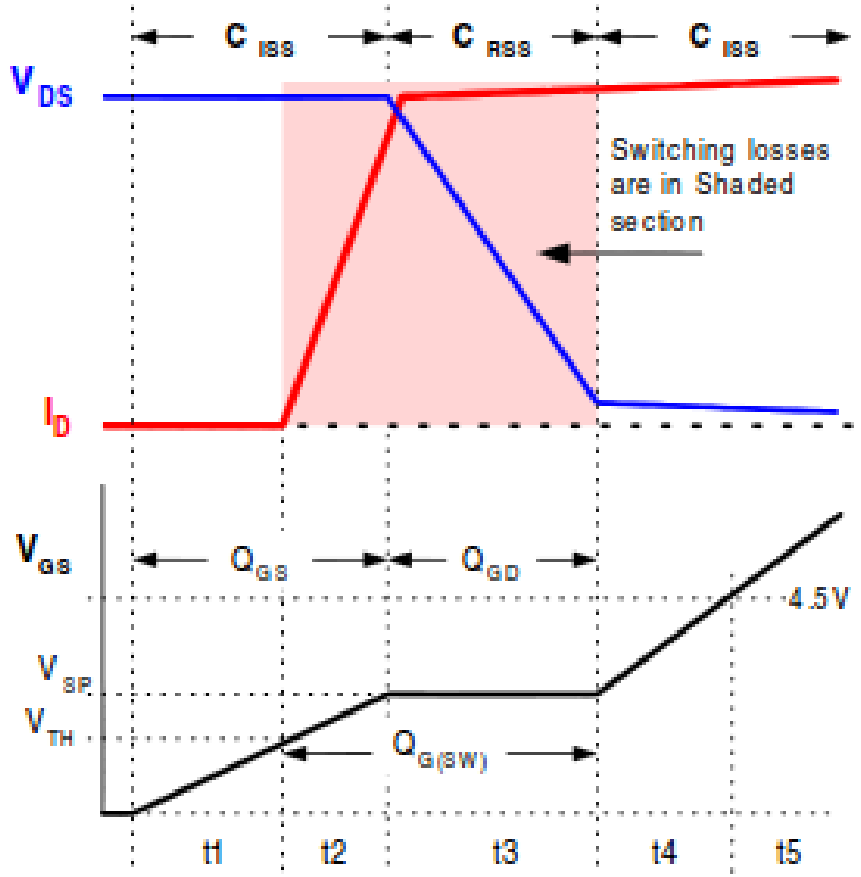


Driving Devices – MOSFET Switching Model

- Recall: You want to fill the capacitor as quickly as is reasonable
- Important datasheet numbers:
  - **Q_g** (typ. nC), **C_{iss}**, **C_{rss}**
  - **$R_{ds\text{-}on}$**

DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		195		pF
C_{oss}	Output Capacitance			135		pF
C_{rss}	Reverse Transfer Capacitance			48		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn - On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Turn - On Rise Time			13	25	ns
$t_{d(off)}$	Turn - Off Delay Time			13	25	ns
t_f	Turn - Off Fall Time			4	10	ns
$t_{d(on)}$	Turn - On Delay Time	V_{DD} = 5 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Turn - On Rise Time			32	60	ns
$t_{d(off)}$	Turn - Off Delay Time			10	20	ns
t_f	Turn - Off Fall Time			5	10	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 1.7 A, V_{GS} = 5 V		3.5	5	nC
Q_{gs}	Gate-Source Charge			0.8		nC
Q_{gd}	Gate-Drain Charge			1.7		nC

Always be aware of what conditions the manufacturing is testing under. Many parameters change with **V_{DS}**.



$C_{ISS} = C_{GS} + C_{RSS}$

Figure 3. High-Side Switching losses and Q_G

Driving Devices – MOSFET Switching Model

- There is actually no *quick* estimate which is accurate for all circumstances.
- One approximation is $\mathbf{t_{sw} \approx 2.2\ R_{gate} * (C_{iss} + C_{rss})}$
  - **Reason: This is the "Rise Time" of a 1st order RC circuit from 10% to 90%.**
- Another uses the charging of $\mathbf{Q_g}$ (total gate charge)

  $\mathbf{t_{sw} \approx (Q_g * R_{gate})/ V_{gs}}$ – tends to underestimate by 33% or so
  - **Reason: This is a linear approximation of a first-order RC circuit charging curve. It will reach 100% quicker than the equivalent differential equation.**

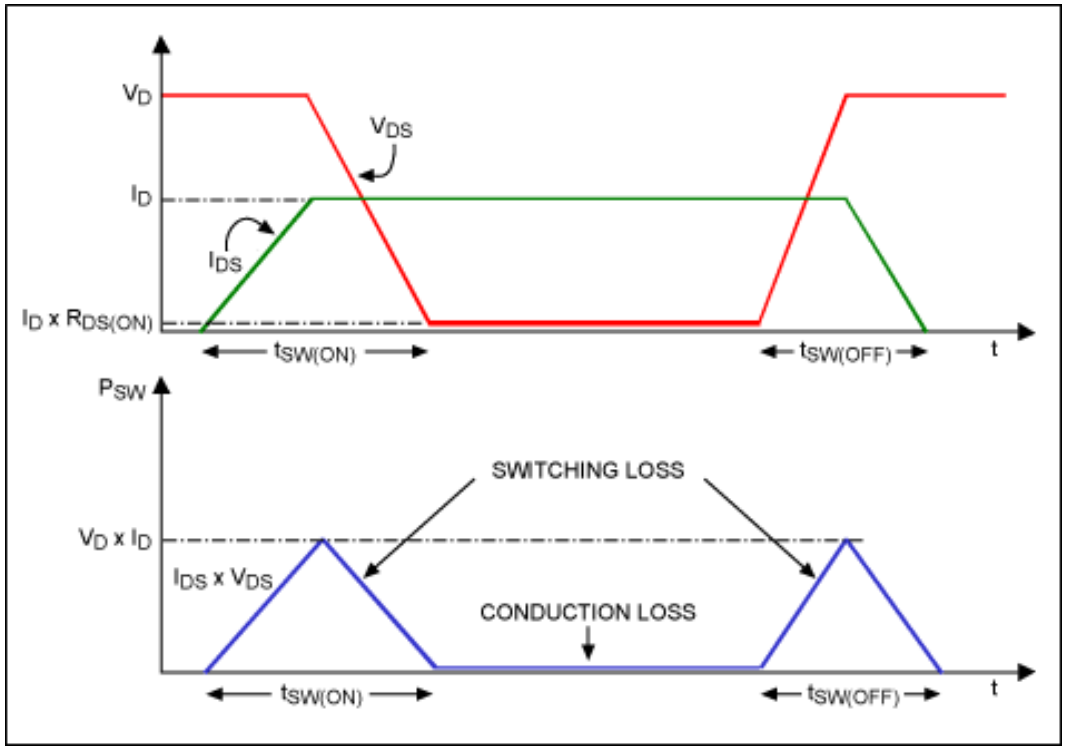
Case study from known result:
Vgs = 15v, Rgate = 10 Ω, Qg = 240nC, (Ciss + Crss) = 9800pF

Method 1: 215 ns (about right)
Method 2: 160 ns (25% optimistic)

Great reading: http://www.vishay.com/docs/73217/73217.pdf
http://www.microsemi.com/document-portal/doc_view/14697-making-use-of-gate-charge-information-in-mosfet-and-igbt-data-sheets

Driving Devices – MOSFET Switching Model

- Characterizing $\mathbf{t_{sw}}$ allows you to choose gate drive components like $\mathbf{R_{gate}}$ and your choice of gate drive voltage $\mathbf{V_{gs}}$.
- Also allows estimation of switching losses for resistive loads.
- For inductive and back-EMF loads like motors, it allows a “worst case” look at switching losses.



$$P_{switching} = \frac{V_{s(off)} \times f_s}{2} \times \left[t_{on} + t_{off}\right] \times I_{on}$$

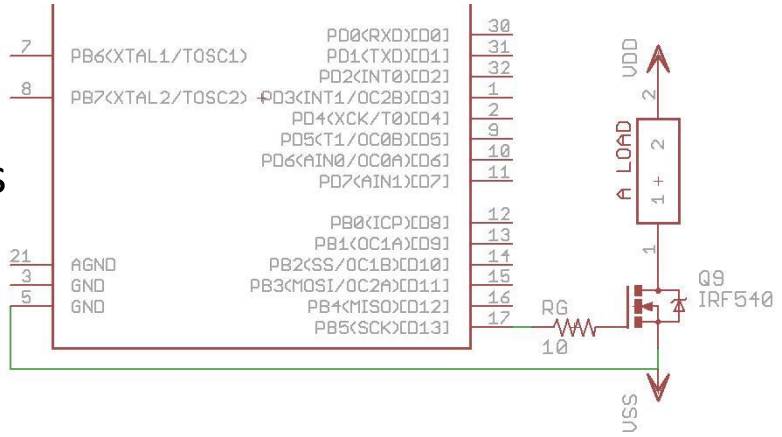
$$P_{on} = D \times I_{on}^{\ 2} \times R_{ds}$$

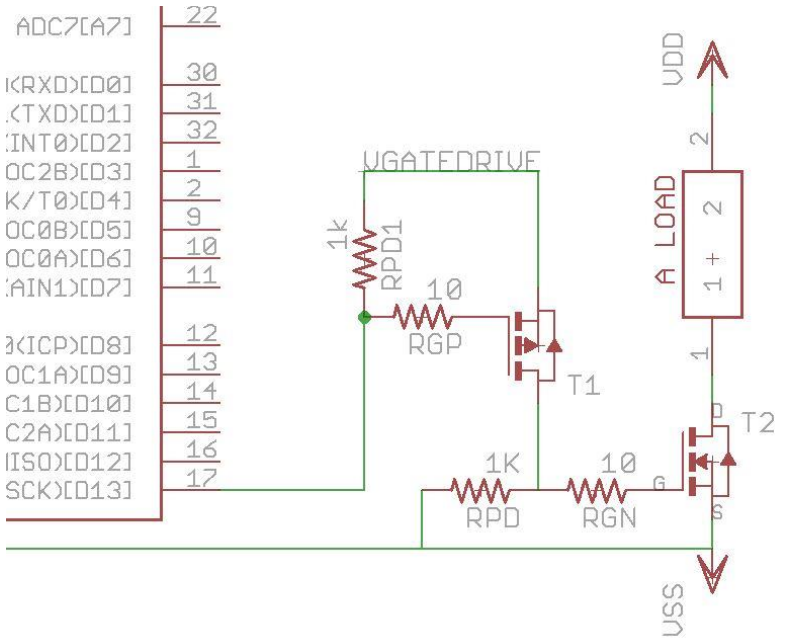
$$P_{total} = P_{switching} + P_{on}$$

$$\eta = \frac{P_{in} - P_{total}}{P_{in}} \times 100$$

Driving Devices – N channel FETs

- Takeaway: Wimpy gate drive will result in large switching loss
- Example 1: Direct microcontroller drive (V_{gs} ≈ 5v max)
  - Might be fine for “just on and off”, no PWMs
  - Microcontroller pins are often 100+ ohms impedance
  - $V_{gs} \approx V_{th}$ will mean actual “turn-on” will take much longer than estimates.
- Example 2: Microcontroller with small P-channel assist
  - Pch directly drops V_{drive} (10-15v) onto the gate.
  - Discharge of both is through a pulldown resistor – this means long **turn-off** times.
  - Low R_{pd} values could mean higher power consumption during high duty cycles.
  - MC pin has to be “LOW” or “HIGH-Z”, else V_{drive} and logic power get connected…

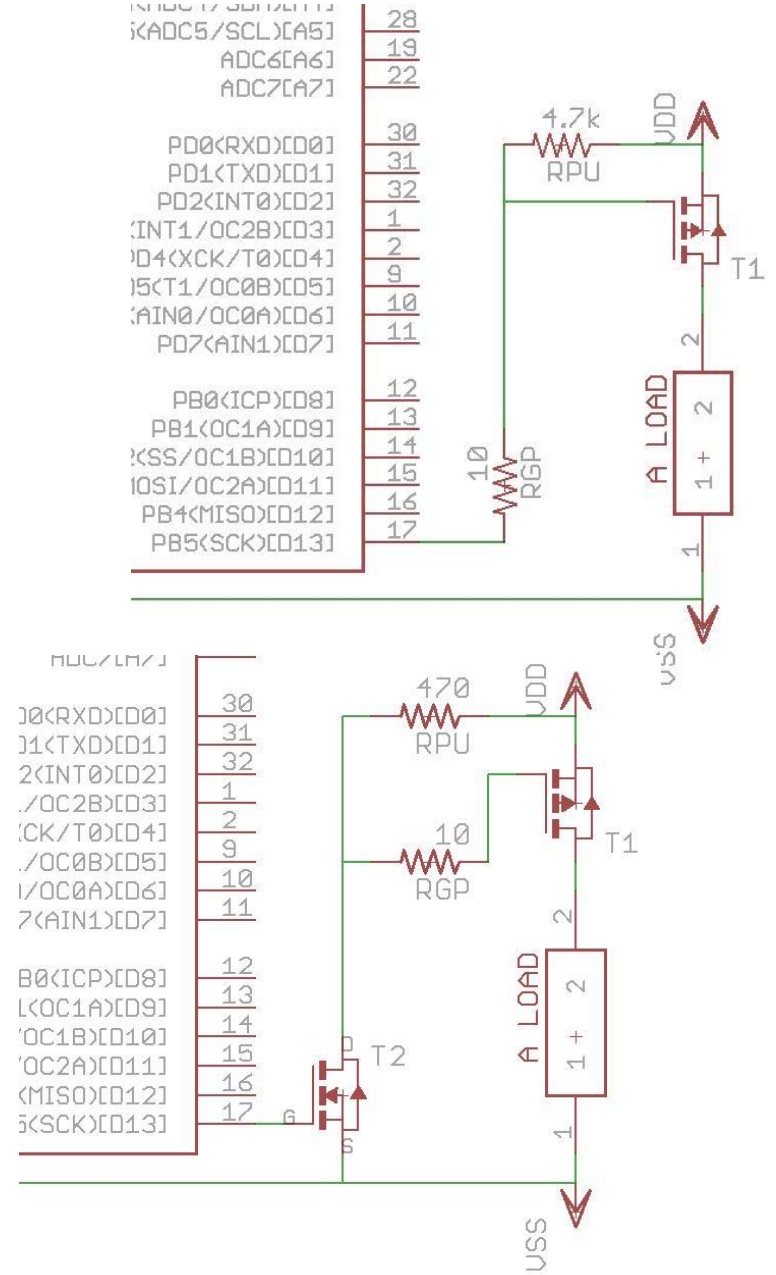




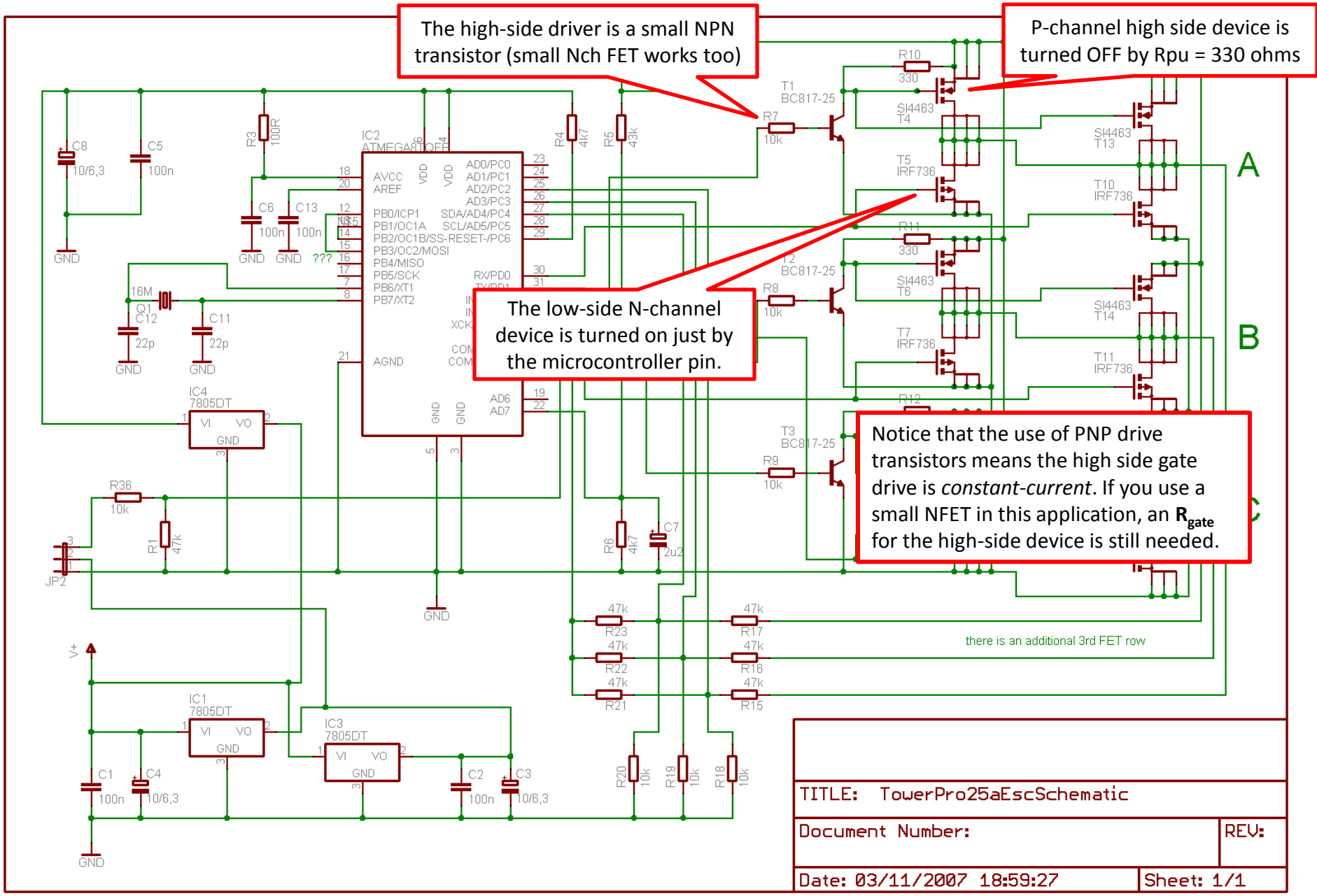
Driving Devices – P channel FETs

- Example 1: Direct microcontroller drive ($V_{gs} < V_{gs,max}$)
  - Again, fine for “just on and off”
  - Turn on: through MC pin pulling LOW
  - Turn off: through **Rpu** (slow).
    Rpu must be large value (kΩs) to prevent damage to MC pin.

- Example 2: With small N-channel assist
  - Actually not bad. MC can switch small N-channel quickly, but turn-off through **Rpu** can still be slow (or high power consuming)



Example P and N Commercial Implementation

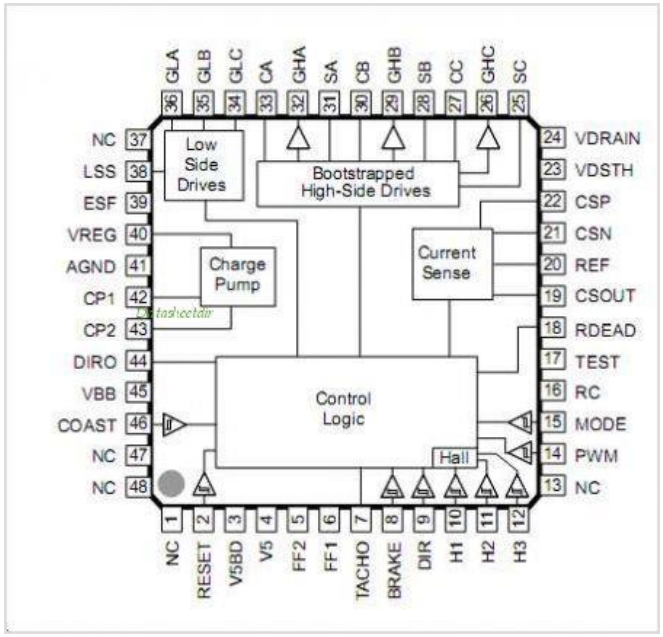


Driving Devices – Gate Drive ICs

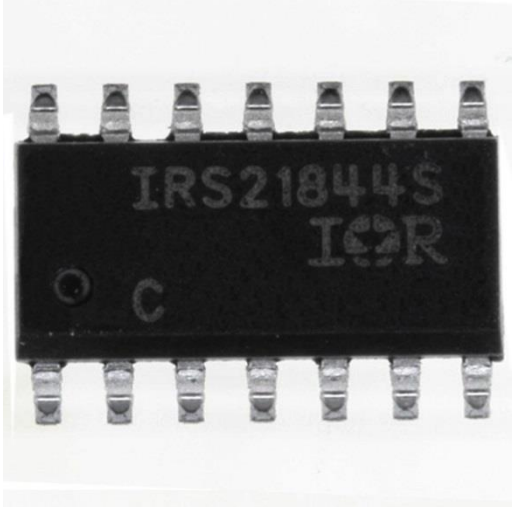
- Take care of most issues for you
  - Shorter turn on and turn-off times
  - Above-VDD supply for NFET high-side
    - Bootstrap; Charge Pump
  - “Dead-time” generation
- **Allows isolation between power ground and logic ground.**
  - Discrete, direct-microcontroller circuits mix grounds and can suffer from noise.

IR2101, a 130/270mA halfbridge driver

IR2125, a single driver that can act as both high- or low-side



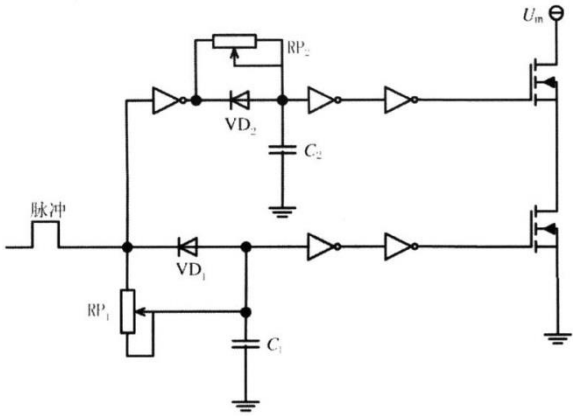
Allegro A3930, a highly integrated 3-phase gate driver.

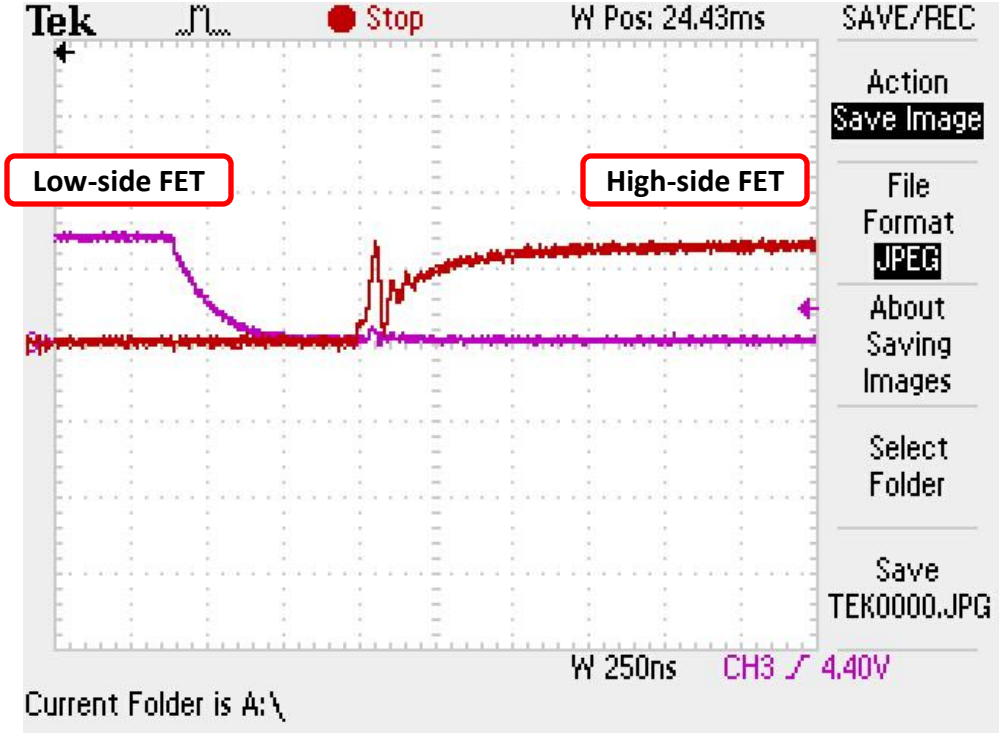


IRS21844, a half-bridge driver with adjustable dead-time

Driving Devices – Deadtime

- All Half-Bridge configurations must have a way to generate **deadtime** in the driver
- Deadtime: Turn one device off BEFORE turning the other on. Typical gaps: 50-200ns
  - **This is far too fast for most inductive loads to be a problem, though too much deadtime or high-current low-inductance loads will cause voltage spikes**
- Many discrete solutions; GDICs usually have it built in.
- Can be done in software
- Newer MCs have it as a periph.

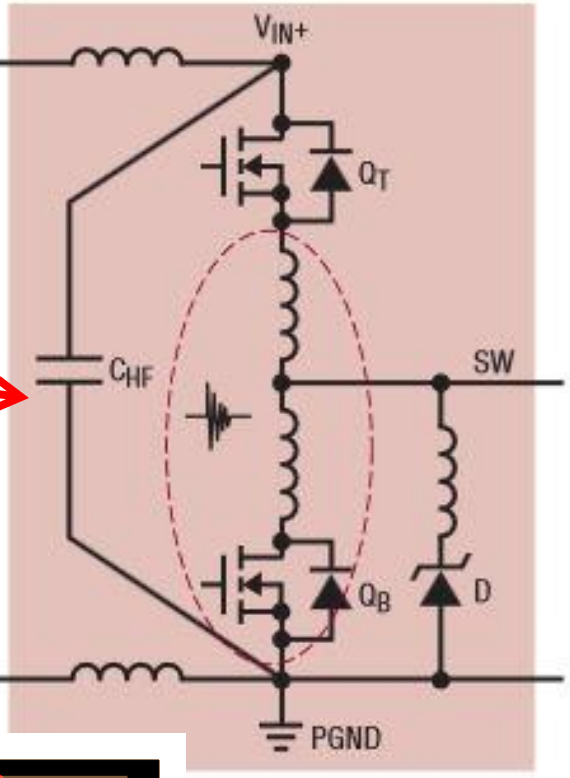




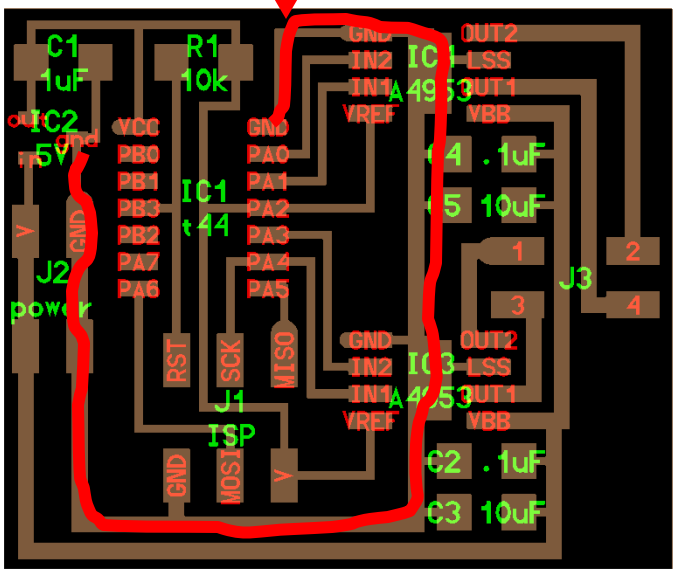
Board Layout Good Practices

- Layout might be more important than part choice.
- **Basic rules:**
  - Use planes and polygons
  - Reduce high dV/dt **areas** and keep signals away from them
    - **Capacitative coupling of noise. What is two big parallel plates? A capacitor!**
  - Reduce high dI/dt **loops**
    - **Inductive transients**
  - Keep your grounds in a tree topology
    - **Eliminate "ground loops"**

High- dI/dt "hot loops" – any signals or sensitive microcontrollers caught in the loop will be cooked, or at least interfered with.



The microcontroller is last in line after the switches to get power! Any more amps and this board might just reset.



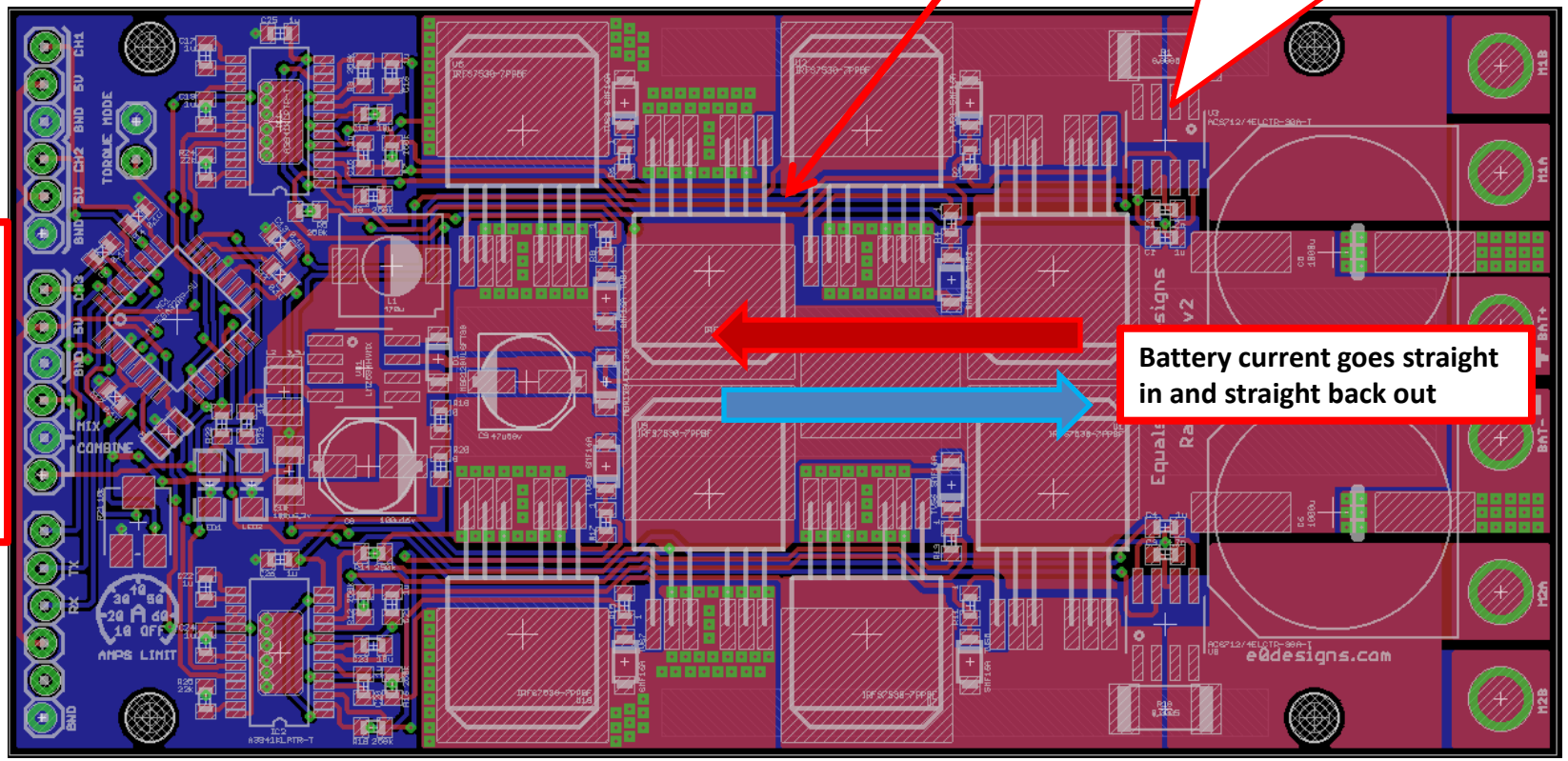
Board Layout Good Practices

- High dv/dt area: Next to big switches Inside a loop containing a switch and bulk capacitor
- High di/dt area: Inside switching current or return current paths

The analog signal trace is surrounded by "Guard traces" connected directly to 5V logic and the logic ground – low impedance to absorb transients, and heavily filtered at the sensor.

This analog current sensor is in the "hot zone", but other measures have been taken to ensure signal integrity.

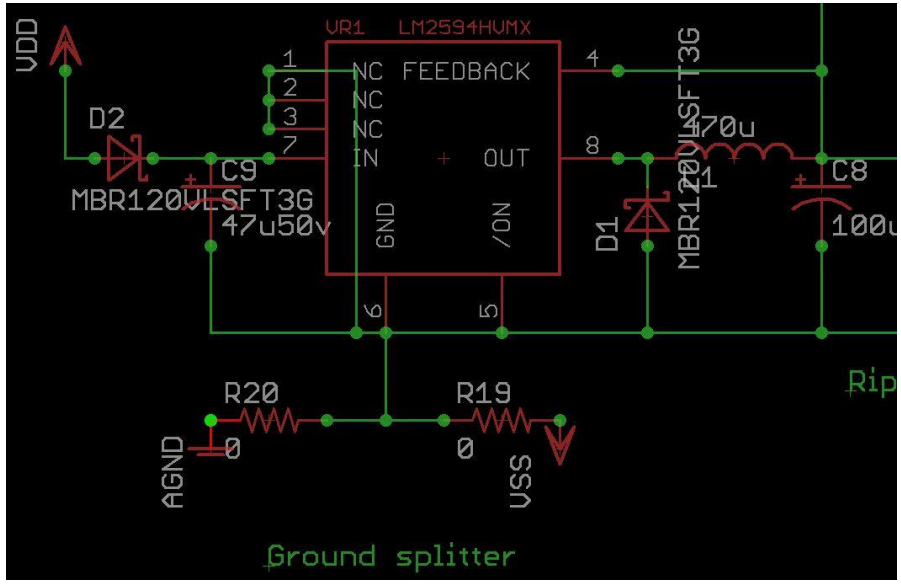
Logic on this board is out of the way of high powered switching

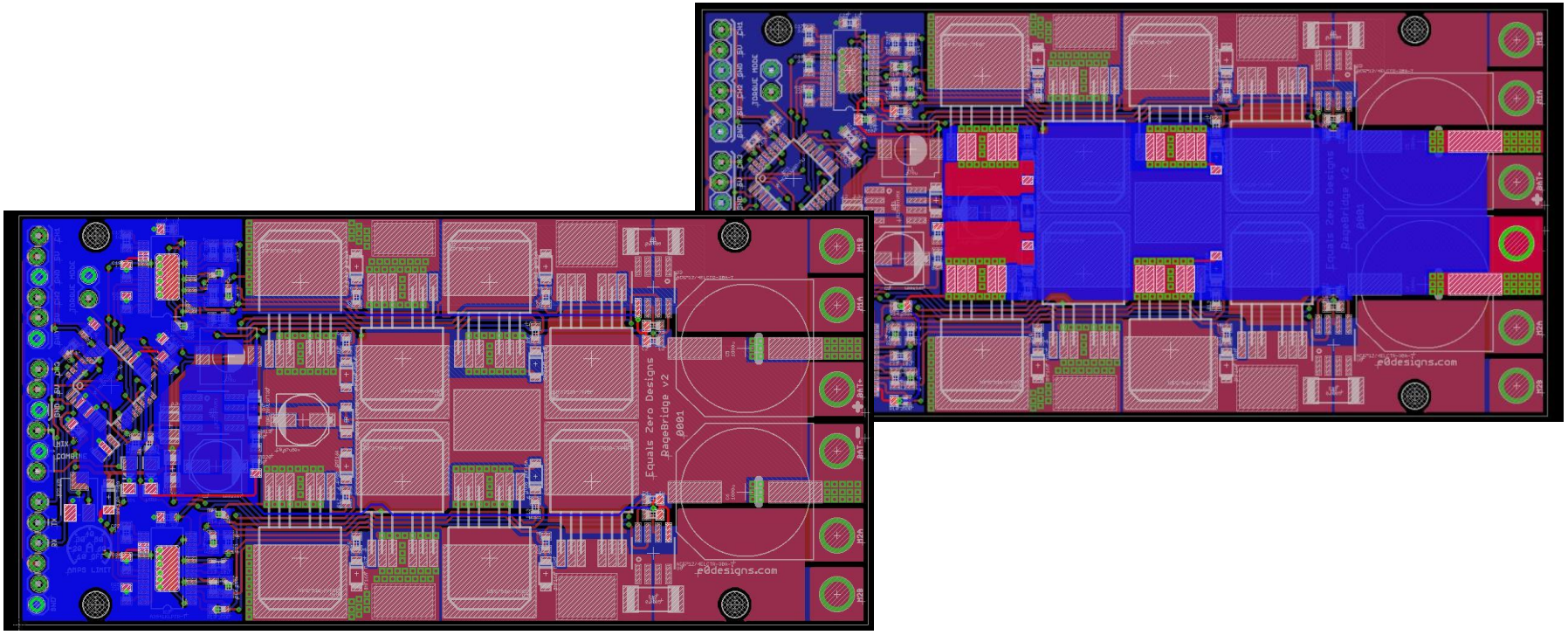


Good reading: http://www.ti.com/lit/ml/slua366/slua366.pdf

Groundskeeping

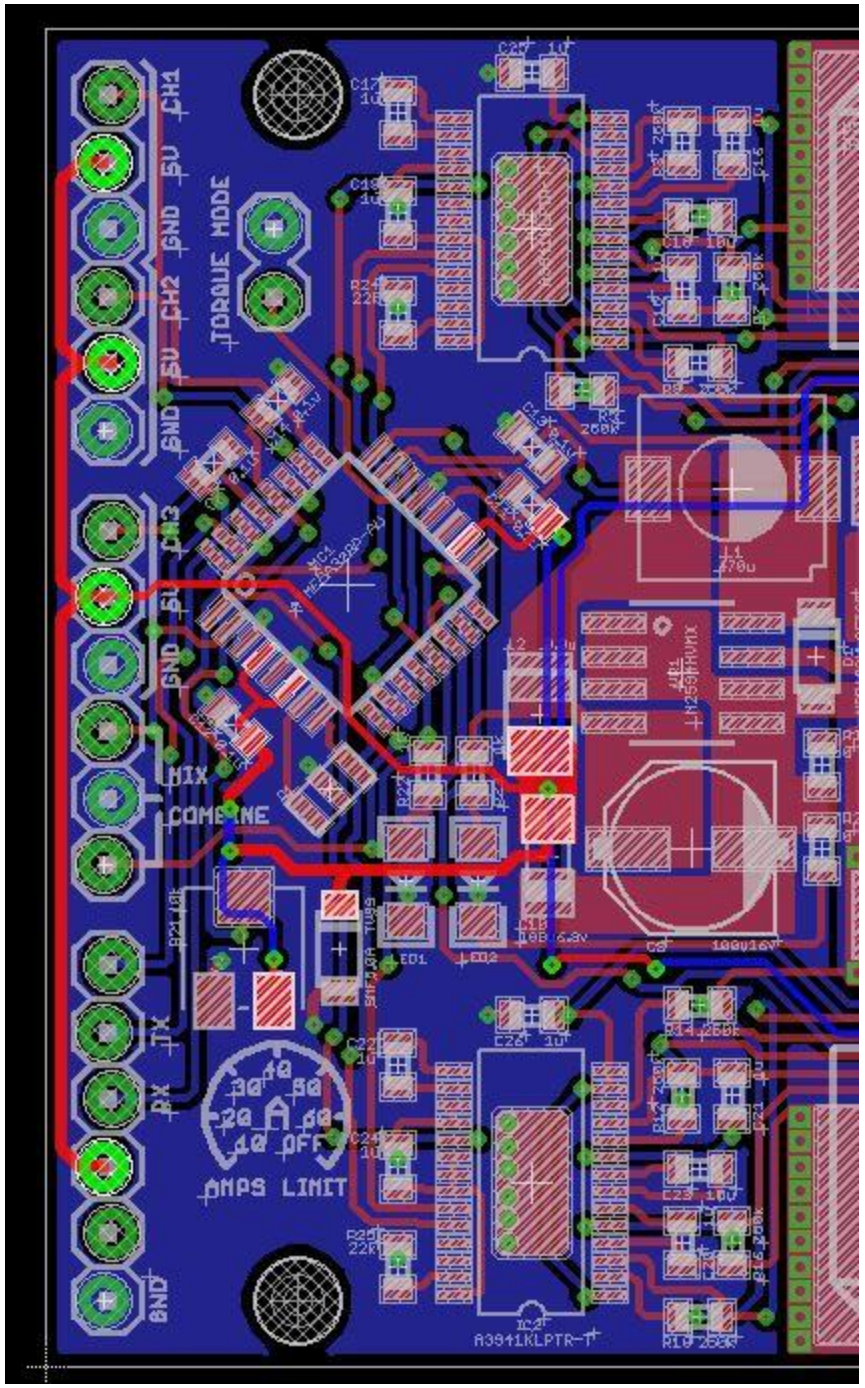
- Not mowing the lawn, but ensuring the separation of **Logic ground** and **power ground.**
- Logic: Serves MC, sensors, inputs
- Power: Serves big power & gate drives only
- Keep them named separately, e.g **AGND** vs. **VSS**





Groundskeeping

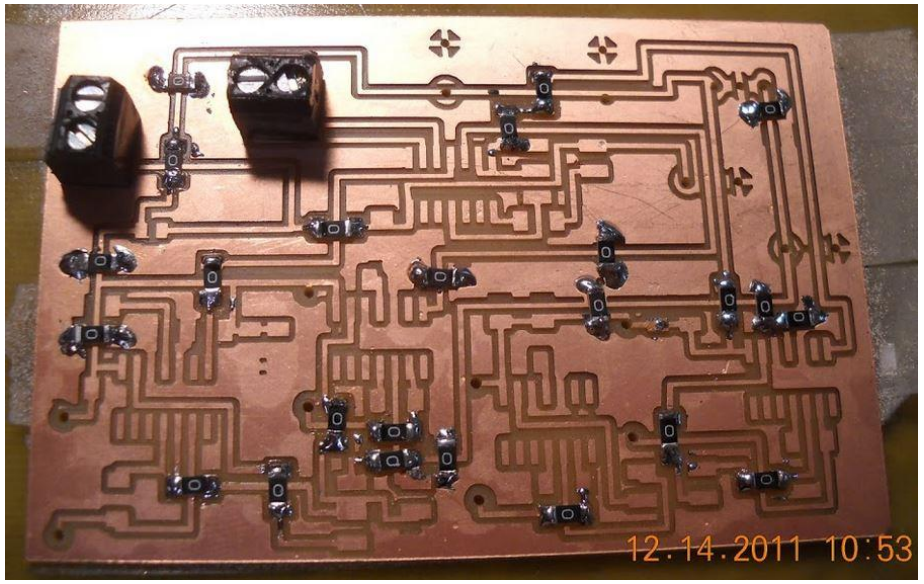
- Ensure your power distribution for all circuits is a star, tree, or line… not loops.
- Place your logic in the cleanest part of said structure; bypass capacitors are your friend.
- Ground plane fill when you can…
  It will save milling time too!
- For FAB boards, you can use a row of 0 ohm jumper resistors to “continue” a plane.



Final Design Considerations

- Select device and drive method based on your needs.
- Static on/off? Almost any will work! Consider $\mathbf{P = I^2 R_{ds\text{-}on}}$ dissipation
- Switching? Consider **turn-on**, **turn-off time**, **switching losses** you can accept
- For thermal dissipation, use $\mathbf{R_{\theta ja}}$ (Thermal resistance, junction-to-ambient)
  - **More complicated and out of scope: Thermal modeling**
- Consider inductive characteristics of your load – will you need a flyback diode?
- Board layout is almost as important (or more important!) than parts alone
- Keep your grounds named and separated, meeting only at 1 point
- Keep sensitive traces away from switching devices
- Bypass capacitors everywhere! Bulk bus capacitance is essential.

- There are some more advanced topics that are out of scope for today.
  - Parasitic inductance and capacitance
  - Detailed modeling of switching time
  - Ripple capacitance, ESR, ESL
  - Gate ringing (is bad) – use $\mathbf{R_{gate}}$ and scope your gate traces; Zener diodes
  - Why to use one gate driver over another – read the datasheet.



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